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10EC46

# Fourth Semester B.E. Degree Examination, Dec.2015/Jan.2016
# Linear ICs and Applications

Time: 3 hrs. Max. Marks:100

**Note:** ***1. Answer any FIVE full questions, selecting atleast TWO questions from each part.***
***2. Missing data, if any, may be assumed suitably.***



## PART – A

1 a. With a neat circuit diagram, explain the basic op-amp circuit. **(06 Marks)**

b. The non – inverting amplifier uses μA 741 op-amp with $R_1 = R_3 = 2.2K$ and $R_2 = 220$ K. Determine maximum possible output offset voltage due to :
i) input offset voltage of 5 mV
ii) input bias current of $I_{B\,(max)} = 500\eta A$
iii) Input offset current of $I_{i(OS)} = 200\ \eta A$
iv) iv) resistance tolerance of ± 10%. **(10 Marks)**

c. Obtain the expression for output voltage for the two input inverting summing amplifier circuit. **(04 Marks)**

2 a. Draw a neat circuit diagram of a capacitor coupled voltage follower and explain its operation with necessary design steps. **(08 Marks)**

b. Design a high impedance capacitor – coupled non–inverting amplifier to have a low cutoff frequency of 200 Hz. The input and output voltages are to be 16 mV and 4V respectively and minimum load resistance is 10 KΩ. Select $R_2 = 1$ MΩ and $C_1 = 0.1$ μF. **(06 Marks)**

c. Explain how the upper cutoff frequency can be set for inverting amplifier with the help of neat circuit diagram and also explain design steps. **(06 Marks)**

3 a. Define loop gain, loop phase shift, pole frequency and phase margin. **(04 Marks)**

b. Explain miller effect compensation. **(06 Marks)**

c. For the circuit shown in Fig. Q3(c), calculate :
i) Full power bandwidth of 1 V peak input and op-amp slew rate of 250 V/μs
ii) Maximum peak output voltage obtain for input signal of 100 KHz and with slew rate of 0.5 V/μs. **(04 Marks)**

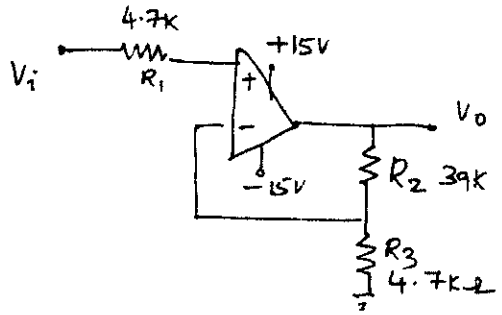


Fig.Q3(c)

d. List the precautions to be observed for op-amp circuit stability. **(06 Marks)**

4 a. Design the current source circuit shown in Fig. Q4(a) to produce a 100mA output to a 40 Ω load. Use a ± 12V supply and an LM 108 op-amp. **(06 Marks)**

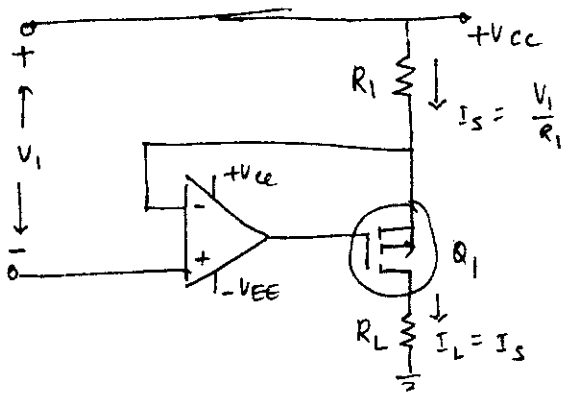


Fig.Q4(a)

b. Sketch the circuit of a current amplifier with floating load. Explain circuit operation and derive an equation for current gain. **(06 Marks)**

c. What are the advantages of precision rectifier over ordinary rectifier? Explain the working of a full wave precision rectifier. **(08 Marks)**

## PART – B

5 a. With relevant diagram, explain the operation of negative clamper circuit using op-amp. **(06 Marks)**

b. Design a triangular waveform generator to produce a ±2V, 1 KHz output. Use a ±15V supply. Also calculate the minimum op-amp slew rate. **(08 Marks)**

c. Explain the working of phase shift oscillator using op-amp. **(06 Marks)**

6 a. With relevant diagrams, explain basic inverting and non-inverting comparator circuit with $V_{ref} = 0V$. **(06 Marks)**

b. With a neat circuit diagram, explain the operation of inverting Schmitt trigger circuit and discuss the design procedure. **(10 Marks)**

c. Using 741 op-amp, design the first –order active low-pass filter to have a cutoff frequency of 1.2 KHz. **(04 Marks)**

7 a. Briefly explain the standard representation of 78XX series 3–terminal IC regulators and enumerate the characteristics of this type of regulators. **(08 Marks)**

b. With the help of neat diagram, explain the operation of adjustable regulator using fixed 3–terminal regulator. **(06 Marks)**

c. Explain the operation of basic high voltage regulator using IC 723. **(06 Marks)**

8 a. Explain the operation of a mono – stable multivibrator using 555 IC timers. **(06 Marks)**

b. Explain the operation of phase – locked loop (PLL) with the help of neat block schematic diagram. **(08 Marks)**

c. What output voltage would be produced by DAC whose output range is 0 to 10 V and whose input binary number is

i) 10 (2 bit DAC)

ii) 0 1 1 0 (4 bit DAC)

iii) 1 0 1 1 1 1 0 0 (for 8 bit DAC). **(06 Marks)**

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